SE/IV/COMP+AI&DS+CSE/C-Scheme/DEC-24/13-12-24

Duration: 3hrs **[Max Marks:80]**

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 Attempt any FOUR [20]

a Explain the minimum mode of 8086

b Explain in brief cache organization of Pentium processor

c Write an assembly language program for 8086 to exchange contents of two memory blocks

d Explain the following instructions: XOR, NOP related to 8086.

e Discuss in brief the Segment Register of 80386DX

2 a Explain the implementation of Paging in Protected mode of 80386. [10]

b Explain the modes of 8255 with proper diagram of each modes [10]

3 a Design 8086 microprocessor-based on following Specifications: [10]
1. MP 8086 working at 10MHz minimum mode.
2. 16 KB DRAM using 4 KB Devices
3. 32 KB SRAM using 8KB chips

b Explain what is ISR? How does 8086 decide the priority of interrupts? [10]

4 a Interface Interrupt controller 8259 with 8086 Microprocessor and modes of 8259. [10]

b Write an ALP for 8086 to reverse a string of 10 characters. [10]

5 a Differentiate between Memory Mapped I/O and I/O mapped I/O. Explain in brief address decoding Techniques [10]

b Explain MESI protocol [10]

6 a Draw the timing diagrams for Read and Write operations in minimum and maximum mode [10]

b Explain hyper threading technology and its use in Pentium 4 [10]

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